Sun	day, 3 December 2023	(Oral Sessions)	(Oral Sessions)	(Oral Sessions)	(Oral Sessions)	(Oral Sessions)	(Fusier Sessions)			
ıy 0.	8:00-17:30			Tutorial 4 most 4	Tutorial 2 part 4	1	Registration Desk			
	9:00-10:30 10:30-11:00			Tutorial 1 - part 1	Tutorial 3 - part 1					
	11:00-12:30			Tutorial 1 - part 2	Tutorial 3 - part 2					
Day	12:30-14:00 14:00-15:30			Satellite WS - part 1	Ī	Tutorial 4 - part 1	1			
	15:30-16:00					-	Coffee Break			
	16:00-17:30			Satellite WS - part 2		Tutorial 4 - part 2				
DAY 1										
	8:00-20:30						Registration Desk			
	9:30-9:40	Opening Ceremony								
		Once les Lestons								
	9:40-10:40	Opening Lecture Mehmet Toner								
_										
053	10:40-11:00	Coffee Break								
7										
J S	11:00-12:40	O 1: Modulators	O 2: Bio-Medical, Bio-Inspired CAS	O 3: SS2 - SS2: Hypercomplex NNs for CAS	O 4: Amplifiers	O 5: EDA: Test and Reliability	Demo & Industry			
ΙĒ				for CAS						
'Monday, 4 December 2023				LUNGU Const	a Hall (3rd Floor)					
	12:40-14:00			LUNCH - Cupoi	a Haii (3 <sup>-2</sup> Floor)	ı				
	14:00-15:40	O 6: A/D Converters I	O 7: FPGA Applications II	O 8: SS1 - SS1: Neuromorphic Devices, Circuits and Systems I	O 9: Energy-Efficient Circuits & Systems	O 10: EDA: Tools, Design, Optimization	POSTER 1: Embedded Micro/Systems & Sensors + 2 ONLINE POSTER			
				Devices, encure and eyelemen	oyotomb	opumeuton.	G GOIDGIS * 2 GILINE ! GG LIK			
	45.40.40.00			2 "	Prook					
	15:40–16:00	Coffee Break								
	16:00–17:40	O 11: A/D Converters II	O 12: Neural Networks II:	O 13: SS1: Neuromorphic Devices,	O 14: Analog & Digital CAS	O 15: Digital Circuits and Systems:	POSTER 2: EDA & Low-Power, Low-			
		2 2 20	Machine/Deep Learning	Circuits and Systems II	Applications	Logic Cells	Voltage Systems			
	19:00-20:30	Welcome Cocktail								
	8:00-16:40	DAY 2								
	0.00 10.40	Registration Desk								
		Invited Lecture								
	9:00-09:50	Burak Göktürk								
	09:50-10:10	Coffee Break								
2023										
	10:10-11:50	O 16: Analog Sub-Circuit Designs	O 17: SS5 - II: Amplifiers	O 18: SS1: Neuromorphic Devices,	O 19: SS3: Defense Industry	O 20: Sensors and Sensing Systems I	POSTER 3: Bio-Medical, Audio, Image, and Video Processing CAS +			
	10.10-11.30	O 10. Analog Gub-Circuit Designs	O 17. 000 - II. Allipliners	Circuits and Systems III	Technologies	O 20. Gensor's and Gensing Gystems i	2 ONLINE POSTER			
ē										
ΙË	11:50-13:30	LUNCH - Cupola Hall (3" Floor)								
ce							POOTED 4: Marking/David Lawrence			
December	13:30–15:10	O 21: Low-Power, Low-Voltage Design	O 22: SS5 - I: Antennas & Filters	O 23: SS1: Neuromorphic Devices,	O 24: Circuits & Systems for Image	O 25: Sensors and Sensing Systems	POSTER 4: Machine/Deep Learning and Other Smart Systems for CAS			
2				Circuits and Systems IV	Processing	II .	Applications			
Tuesday,	15:10–15:30			Coffee	Break					
S				551100						
Lee		0.00: 0		0.00. Marriago (1.0)	0.00, 011 Pro					
1	15:30-17:10	O 26: Circuits & Systems for Communications	O 27: SS5 - III: RF Applications	O 28: Memory Cell Circuits & Systems	O 29: Signal Processing in Circuits & Systems	O 30: Oscillators				
				,	,					
	<b> </b>	Innovation and Start-ups in CAS								
	17:30–19:30	(YPCAS-DEICAS Joint Event)								
DAY 3										
_	8:00-10:00	DAY 3 Registration Desk								
Wednesday, 6 December 2023		Invited Lecture								
	8:30-9:30	Hakkı Kaya Ocakaçan								
		(presenting city tour)								
	9:30-17:00	ICECS 2023 CITY TOUR								
	0.00 17.00	ILEGS 2023 CHT TOUR								
		Gala Dinner & Awards Ceremony								
edu	19:00–21:00									
>										
Ц	L									
DAY 4										
	9:00-16:00						Registration Desk			
က	I	Invited Lecture								
202		Luca Benini								
	9:30–10:40	Luca Beriiiii								
7		Luca Bellilli			Coffee Break					
iber 2	9:30–10:40 10:40–11:00	Luca Defilifi		Coffee	Break					
ember 2		Luca Bermin		Coffee	Break					
ecember 2	10:40–11:00		O 32: Smart Systems for CAS				POSTER 5: Analog/Mixed-			
7 December 2023		O 31: FPGA Applications I	O 32: Smart Systems for CAS Applications	Coffee O 33: Embedded and Micro/Systems	O 34: Phase-Locked Loop Circuits		POSTER 5: Analog/Mixed- Signal/Microwave/Power Circuits			
7	10:40-11:00			O 33: Embedded and Micro/Systems	O 34: Phase-Locked Loop Circuits					
7	10:40–11:00			O 33: Embedded and Micro/Systems						
7	10:40-11:00	O 31: FPGA Applications I		O 33: Embedded and Micro/Systems  LUNCH - Cupoli	O 34: Phase-Locked Loop Circuits					
7	10:40-11:00	O 31: FPGA Applications I  O 35: Linear and Non-Linear Circuits		O 33: Embedded and Micro/Systems  LUNCH - Cupol:  O 37: SS4: Artificial Intelligence Methods for Modeling and	O 34: Phase-Locked Loop Circuits					
Thursday, 7 December 2	10:40-11:00 11:00-12:40 12:40-14:00	O 31: FPGA Applications I	Applications	O 33: Embedded and Micro/Systems  LUNCH - Cupol  O 37: SS4: Artificial Intelligence	O 34: Phase-Locked Loop Circuits					

The Grand Ballroom 3 (Oral Sessions)

Azure Meeting Hall (Oral Sessions) Peridot Meeting Hall (Oral Sessions) Foyer (Poster Sessions)

The Grand Ballroom 1 (Oral Sessions)

15:40-16:00

Closing Ceremony

The Grand Ballroom 2 (Oral Sessions)